# Hardware limitations of sampling and digitisation in data acquisition systems (DAQ)

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# Outline

**Previous seminar**

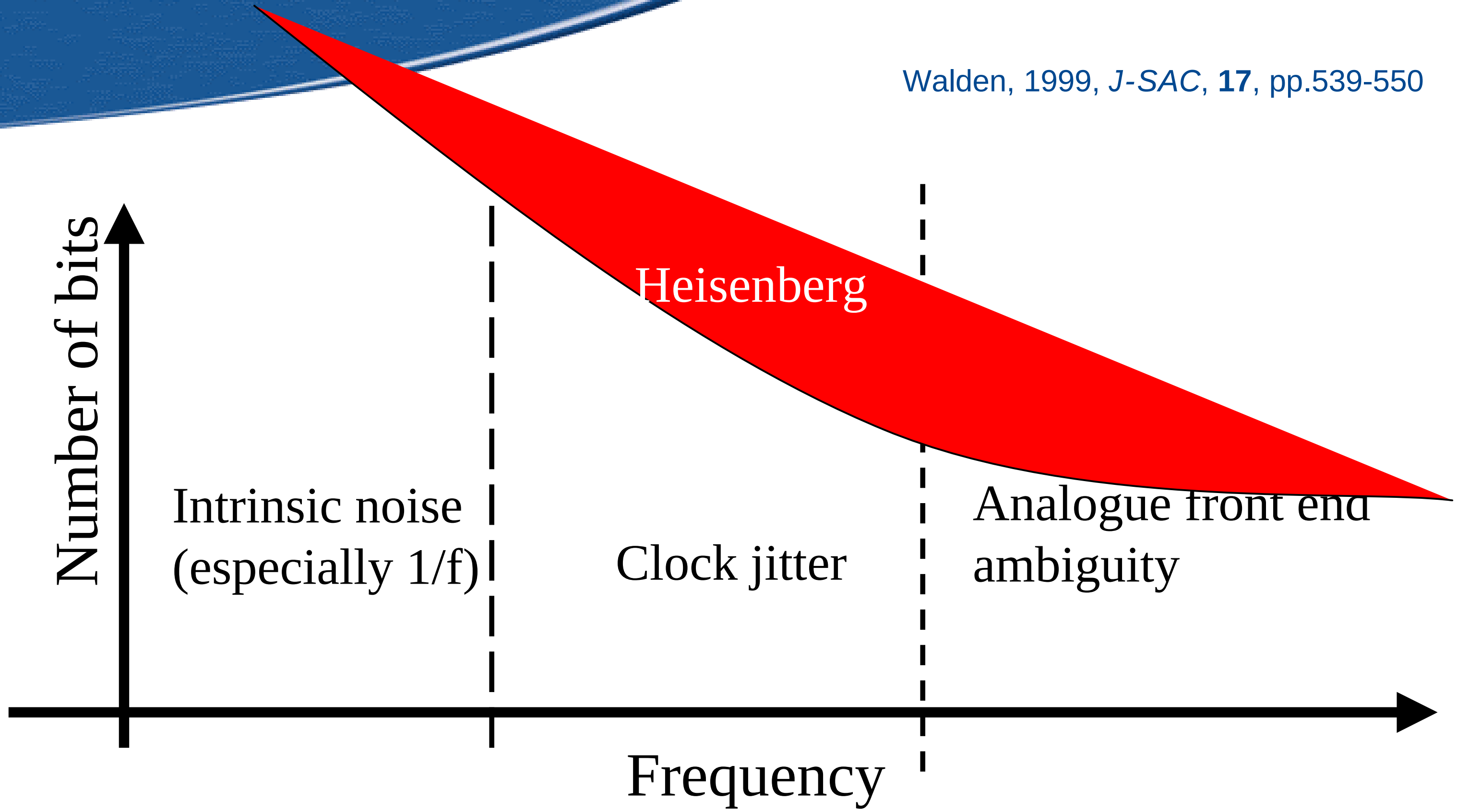
Quantisation error modelling,Quantisation noise of Nyquist and oversampling rate DAQ, DAQ limitations due to quantisation noise modelling, Anti-aliasing filter topologies and errors, effect of sampling rate on the accuracy of a DAQ

**This seminar**

- Analogue to digital conversion
  - Limitations and Technologies
  - Comparison
- DAQ limitations and performance improvements
  - Analogue electronic components
  - Digital hardware
  - System design
- Conclusion
  - Checklist for accurate digitisation

# Limitations of ADC technologies

Walden, 1999, *J-SAC*, **17**, pp.539-550




Werner Heisenberg: It is not possible to make a simultaneous determination of the energy and the time coordinate of a particle with unlimited precision

$$\Delta E \ \Delta t \geq \hbar$$

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# ADC technologies

- Integrating converters (dual ramp)
- Delta Sigma

High resolution, low speed

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- Successive approximation (SAR)
- Switched capacitor
- Voltage-to-frequency converters

Medium resolution, medium speed

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- Pipeline
- Flash (parallel encoded)

Low resolution, high speed

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- Combination of the above in interleaving mode

Precision ADC: Not integrated circuits but discrete components on a PCB

Fast ADC: integrated circuits

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# Comparison

| Topology | Resolution (bits) | Sampling rate (samples/sec) | Linearity | Multi-channel | S/H? (signals <1MHz) |
|---|---|---|---|---|---|
| Flash | 8-12 | 500 M | ✓ ✓ ✓ ✓ | ✓ ✓ ✓ ✓ | No |
| SAR | 8-16 | 1 M | ✓ ✓ | ✓ ✓ ✓ | Yes |
| Delta-Sigma | 12-24 | 50 k | ✓ ✓ ✓ ✓ | ✓ | No |
| Dual-ramp | 16-26 | 1 k | ✓ ✓ ✓ ✓ | ✓ ✓ | Yes |

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# Errors in multi-channel DAQ

- Switches → Relays (solid-state, reed relays) / Analogue switches (FET - semiconductors)
- ON resistance ($R_{ON}$)
- $R_{ON}$ function of input voltage (semiconductors)
- Parasitic capacitance
- Cross-talk between channels
- Charge injection (semiconductors)
- More than two channels connected at the output of the multiplexer
  - Use a voltage-to-current converter $\rightarrow$ switch $\rightarrow$ current-to-voltage converter
  - Use a switch with low charge injection or opto-FET
  - Break-before-make

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# Practical limitations due to component and system design

- ✓ Reference voltage
  - ❑ ADC relates the input signal to a reference voltage
  - ❑ The reference voltage noise, time and temperature drift introduce error
  - Use a reference voltage with low noise, time and temperature drift
- ✓ Power supply
  - ❑ Power supply has ripple and noise
  - ❑ Ripple can be coupled to the input signal and electronic circuits
  - ❑ Ripple change the offset value of electronics of the data converter
  - Use a power supply with low ripple and a converter with good PSRR
  - Use a linear power supply for the analogue part and a switching mode for the digital
- ✓ Connections to the computer
  - ❑ Noise (switching mode power supplies)
  - ❑ Common mode signals (ground)
  - Use filters and digital isolators

# Practical limitations … (continued)

- ✓ Clock jitter (jitter in the time domain - phase noise in the frequency domain) (standard deviation of the sample instant in time)
  - ❑ Use a low jitter clock and data converter
  - ❑ Avoid using multiplexers and optocouplers on the clock line
  - ❑ Terminate clock line if its length is greater than $t_r/(6 \times \text{Delay})$

  $t_r$:rise time of clock, Delay: propagation rate of the signal on the board, 6 ps/mm for FR4
- ✓ Coupling of signals (analogue or digital)
  - ❑ Locate the clock as close as possible to the ADC
  - ❑ Keep digital circuits away from the analogue
  - ❑ Minimise area overlap between analogue and digital circuits
- ✓ Floating internal nodes due to unconnected digital pins

  Do not leave unused digital pins unconnected

# Practical limitations … (continued)

- ✓ ADC has finite input impedance with non-constant magnitude frequency response
- ✓ Analogue and digital grounds of components (common mode signals)

  Star connection
- ✓ Fast signals require Sample and Hold (or Track and Hold)
  - ❑ Increase nonlinearity
  - ❑ Noise and offset
  - ❑ Non-flat frequency response
  - ❑ Droop

  Use a faster converter if possible or for RMS measurements convert the AC to DC and sample the DC, use a capacitor with low leakage, careful PCB lay-out, active components with small input current

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# Practical limitations … (continued)

- ✓ Power supply integrity problems
  - ❑ The power supply current is correlated to the ADC output code
  - ❑ Transient currents in the power supplies can introduce noise

  Minimise the current flowing IN and OUT of the digital part of the data converter using buffers and use decoupling capacitors

  *Programming:* minimise the number of external RAM reading/writing

  minimise the number of code lines
- ✓ Analogue electronic components have “memory”, time and temperature drift, frequency response

  Use “good” quality electronic components
- ✓ The PCB is a component and not a mounting surface for components
  - ❑ Frequency dependent dielectric characteristics
  - ❑ Time and temperature drift

  Use a PTFE-like material for precision analogue and FR4 for digital

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# Practical limitations … continued

- ✓ DC offset voltage
- ✓ Thermal EMF
- ✓ Self-heating of components
- ✓ Overheating of components (overloading)
- ✓ Mechanical movements
- ✓ Mechanical stress
- ✓ Dielectric problems (frequency response and leakage)
- ✓ Air drafts / flow
- ✓ Humidity

**Everything else I forgot to mention or I do not know about!**

# Digital hardware

- Digital Signal Processors, Field Programmable Gate Arrays (FPGA), microcontrollers and microprocessors
- Digital Signal Processors
  - Optimised for DSP
  - Harvard architecture
  - Floating point and fixed point arithmetic
  - Internal + external RAM (?)
  - Built-in standard PC interface
  - Limited input / output (I/O)
  - Assembly, C/C++
  - High cost per device
- FPGA
  - Parallel operation
  - Flexible
  - Internal RAM (?)
  - VHDL, System C, manufacturer specific
  - Low cost per device

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# DSP limitations

**DSP limitations**

Numerical errors

Jitter of the sampling rate

- Both of them change the gain of the digital filters or controllers in an unpredictable way
- The upper bound of the error can be estimated

Performance depends on the input data!

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# DSP limitations … (continued)

**Numerical errors**

- Finite wordlength of the registers used for storage
- Finite length of the arithmetic logic unit (ALU)
- Operating system may not utilise the hardware (e.g. a 32-bit operating system running on a 64-bit processor)
- Programming language (integer, short integer) - portability

**Jitter of the sampling rate**

- Jitter of the clock (time and temperature dependent)
- Finite computational time (not well defined)
- Internal clock multiplication
- Input / output: polling or interrupt driven (unpredictable latency)
- Operating system attends housekeeping tasks non-transparent to the user: Real Time Operating Systems give you a worst case time window
- Program structure (programmer's ability)

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# Digital hardware survival guide

***Minimise Interference, Power dissipation, Sampling rate jitter, Numerical errors***

- Power Dissipation : Static (DC) + Dynamic ($\propto CfV^2$)
- Use the slowest possible clock permitted by your application
- Use low count IC packages to minimise stray capacitance
- Use low voltage logic (but too low voltage has less noise immunity)
- Avoid accessing an external RAM – utilise the cache
- Use blocks of data to minimise sampling rate jitter
- Use a clock with non-fast edges to minimise interference
- Long lines needs termination
- Use ground planes – do not mix digital and analogue ground planes
- Use differential drivers for long electrical cables (EMC) – better fibre optic
- Use the minimum number of bits needed to represent a number
- Minimise the number of mathematical operations

# Want accurate digitisation?
# Do your homework

- Understand the terms and test conditions used for the ADC specifications
    - IEEE 1241-2001
    - IEC 62008
- Understand the noise sources of the DAQ
- Investigate whether the noise sources in the system are correlated
- Calibrate the DAQ at the frequencies of interest
- Test the stationarity (time and temperature drift) of your DAQ
- Understand the theoretical limitations of the techniques used (hardware and algorithms)

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# Conclusion

- Mixed signal DSP is not only a mathematical operation
  - System noise (e.g. electronic, interference, quantisation)
  - Sampling jitter
  - Dynamic power dissipation
  - Numerical errors
- Oversampling can reduce only random errors and not bias
- The DSP algorithms are frequency independent but the noise is not
- Using a state-of-the-art DAQ and DSP algorithm does not guarantee state-of-the-art results
- The use of “gold-plated” components does not guarantee high performance, only high cost
- Precision AC DVMs do not use sampling of the AC signal!
- Understand the limitations of the technologies
- People’s ability is important

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