



National Physical Laboratory

Sampling, digitisation and filtering requirements of data acquisition systems

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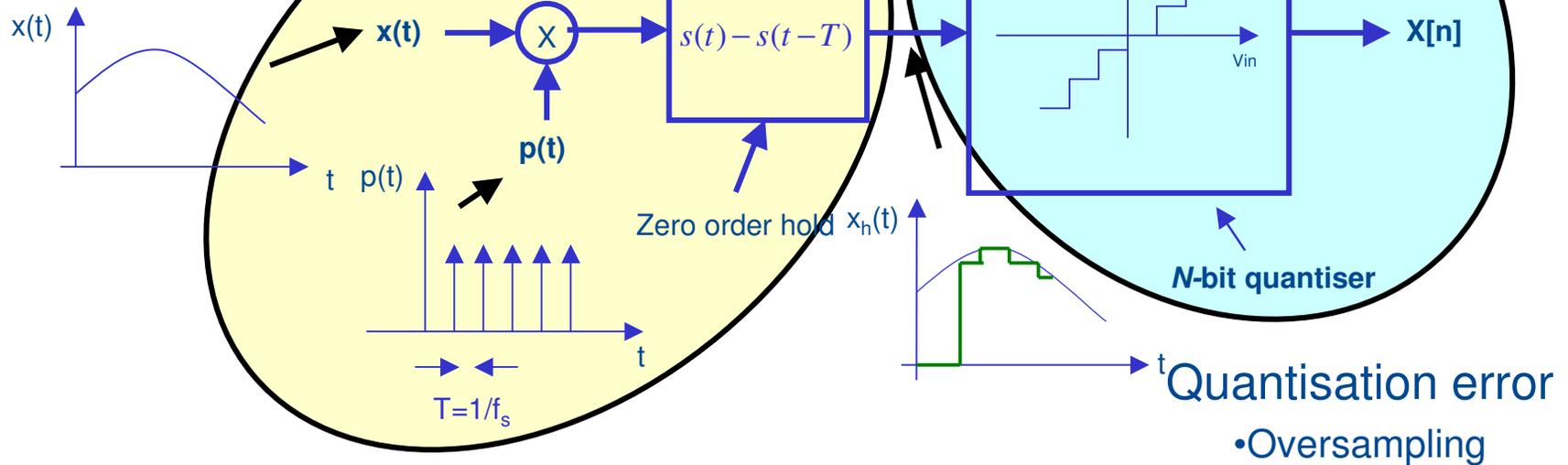
Sampling and digitisation of analogue signals

Sampling theorem conditions

$x(t)$ bandlimited

$$f_s \geq 2f_B$$

$2f_B$ Nyquist sampling frequency



Aliasing

- LPF
- Oversampling

Outline

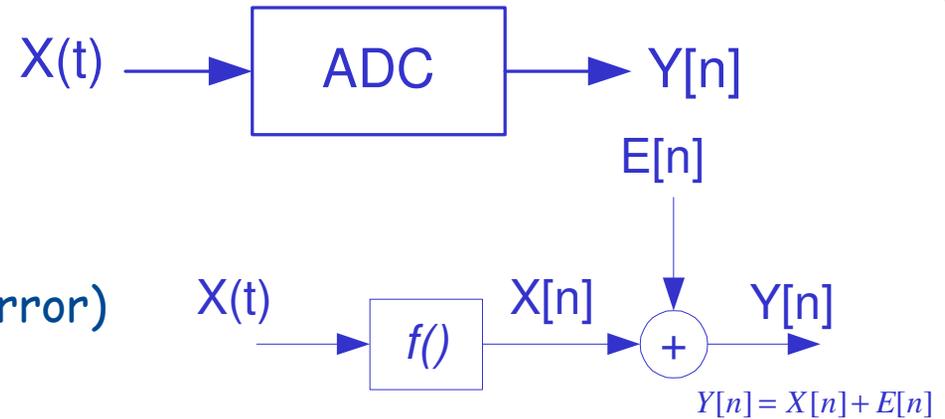
Part I Quantisation error

- Modelling the ADC quantisation error
- Quantisation noise of Nyquist rate DAS
- Quantisation noise of oversampling rate DAS

Part II Low pass filtering

- Filtering requirements of DAS
- Loading effects introduced by filters
- Choosing filter transfer function and topology

Assumptions for the nature of the quantisation error



$X[n]$: input sequence

$E[n]$: error sequence (quantisation error)

WSS: wide-sense stationary

Quantisation error: difference between the value of the analogue input and the analogue equivalent of the digital representation.

Assumptions

- $E[n]$ WSS random process, uniform PDF
- $E[n]$ uncorrelated to $X[n]$
- $X[n]$ WSS random process

WSS: 1st and 2nd statistical moments are independent of the time origin

Quantisation error of ADC

ADC can use either rounding or truncation

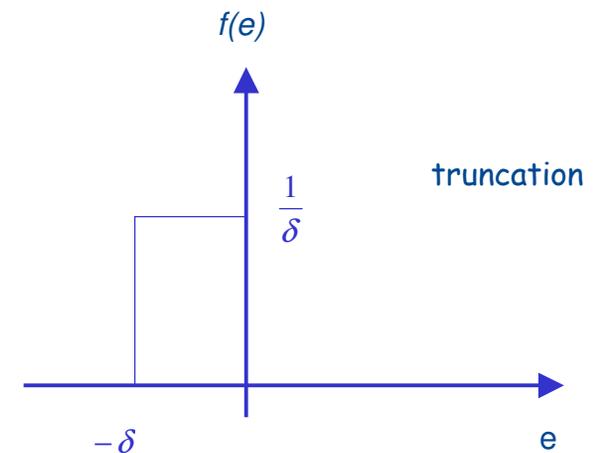
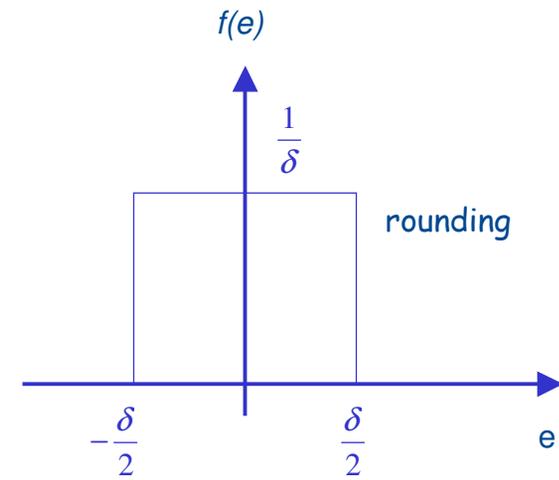
Rounding

$$m_e = \frac{\frac{\delta}{2} - \frac{\delta}{2}}{2} = 0 \quad \sigma_e^2 = \frac{\left(\frac{\delta}{2} - \left(-\frac{\delta}{2}\right)\right)^2}{12} = \frac{\delta^2}{12}$$

Truncation

$$m_e = \frac{0 - \delta}{2} = -\frac{\delta}{2} \quad \sigma_e^2 = \frac{(0 - \delta)^2}{12} = \frac{\delta^2}{12}$$

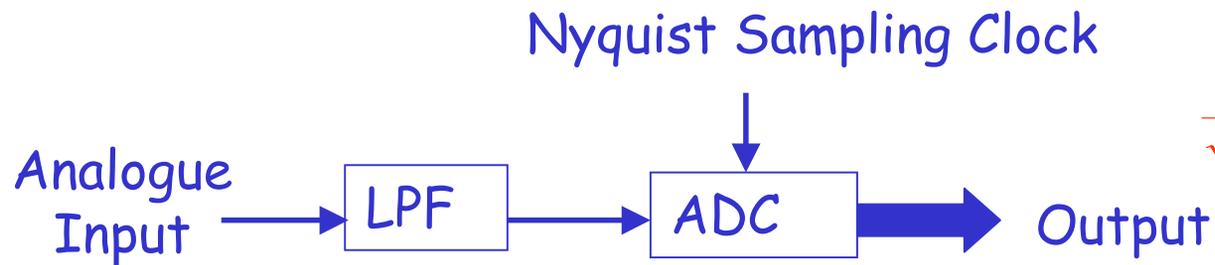
$$\delta \text{ LSB} \quad \delta = \frac{V_{FS}}{2^N}$$



V_{FS} : input voltage span of the ADC

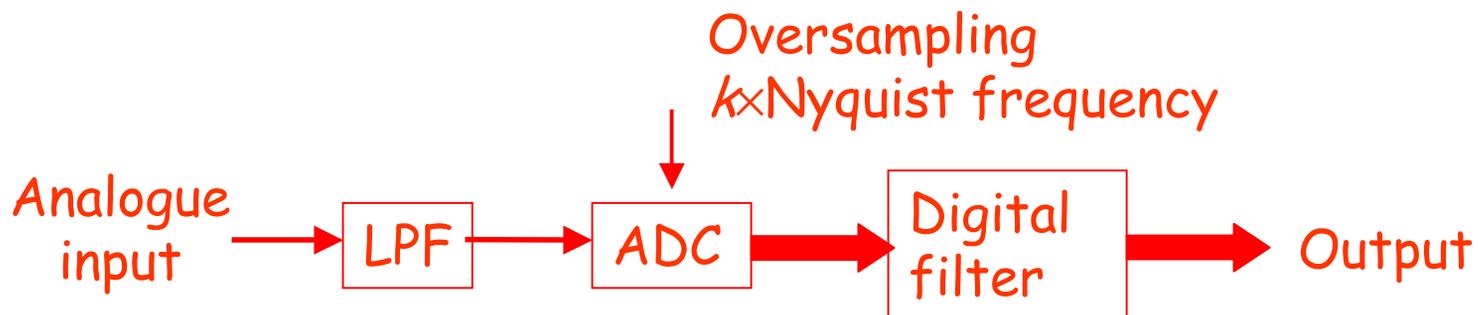
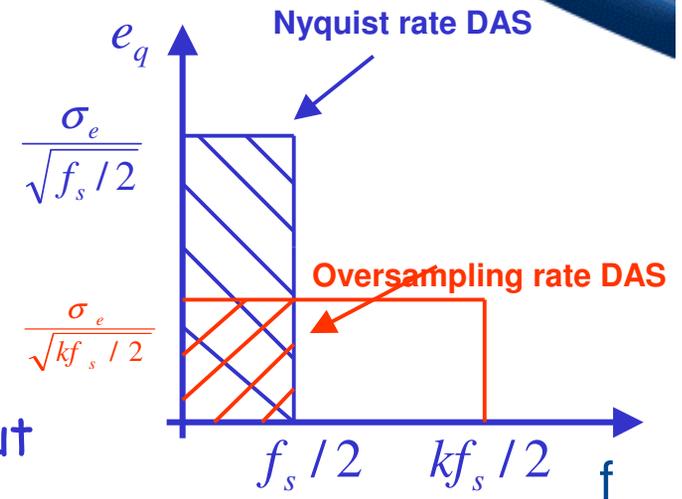
N : ADC number of bits

RMS value of the quantisation noise of DAS



$$e_q = \frac{\sigma_e}{\sqrt{f_s/2}}$$

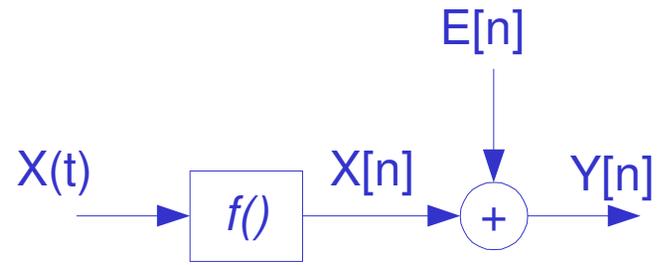
$$E_q = \left(\int_0^{f_s/2} e_q^2 df \right)^{1/2} = \sigma_e$$



$$e_q = \frac{\sigma_e}{\sqrt{kf_s/2}}$$

$$E_q = \left(\int_0^{f_s/2} e_q^2 df \right)^{1/2} = \frac{\sigma_e}{\sqrt{k}}$$

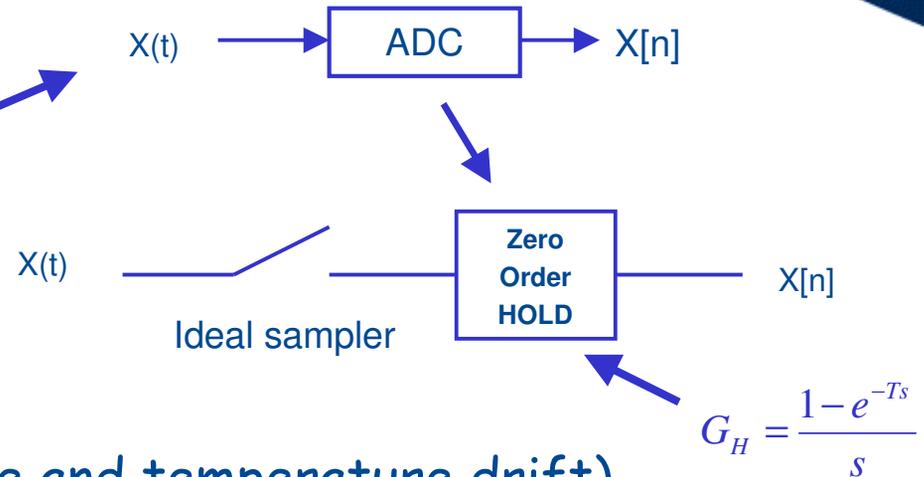
However, ...



- Some signals (e.g. DC and sinewaves) violate the assumption that $X[n]$ is a WSS random process
- The assumption $E[n]$ is a WSS random process with uniform PDF can depend on the DAS topology and components
- The assumption $E[n]$ is uncorrelated to $X[n]$ can depend on the technology of the ADC, topology of the DAS and the $X[n]$
- The above analysis can be valid for deterministic signals with high value high frequency components when "enough" samples are taken

However, ... (continued)

- ADC is not simply
- ADC to operate needs
 - ✓ Power supply (ripple)
 - ✓ Reference voltage (noise, time and temperature drift)
 - ✓ Connections to computer (noise)
 - ✓ Analogue and digital grounds (common mode signals)
 - ✓ Analogue electronic components have "memory", time and temperature drift, frequency response

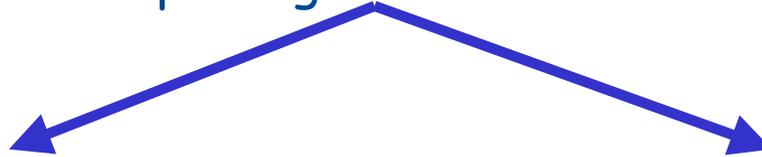


Want accurate digitisation? Do your homework

- Understand the terms and test conditions used for the ADC specifications (IEEE Std 1241-2001)
- Use histogram techniques to measure the ADC noise (measure a "clean" DC signal several times to obtain the histogram)
- Understand the noise sources of the DAS
- Calibrate the DAS at the frequencies of interest
- Test the stationarity (time and temperature drift) of your DAS
- Oversampling can reduce only random errors and not bias
- Dither can help but be cautious
- Precision AC DVMS do not use sampling of the AC signal!

Filtering

- Electronic filtering: modify the content of a signal
- Filter is an operator
- Frequency domain: modify the spectrum (amplitude and/or phase) of the input signal



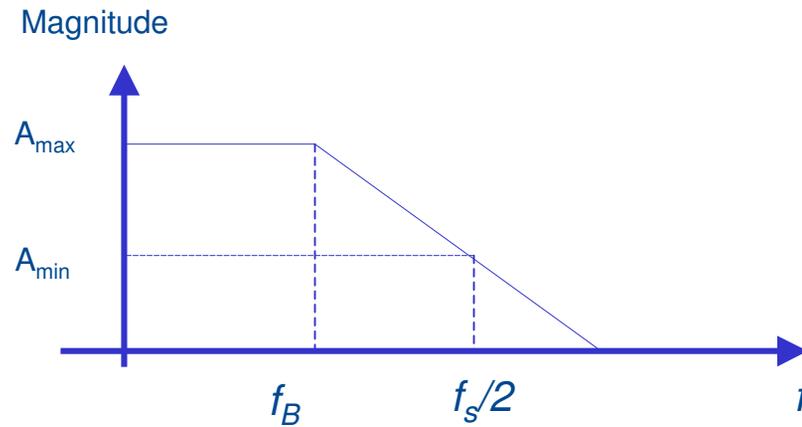
Frequency selective filters

Frequency shaping filters

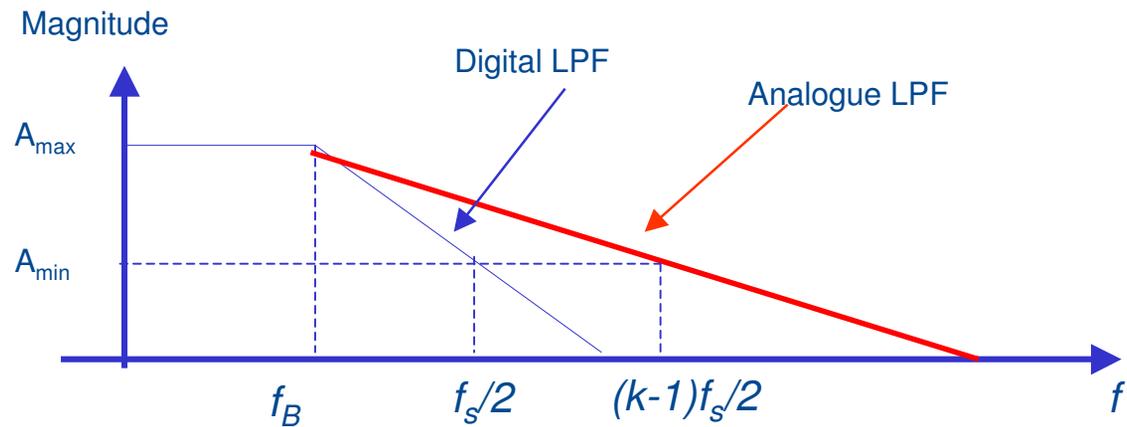
- Anti-aliasing filters → frequency selective filters
- Filters used in DAS: anti-imaging, anti-aliasing, reconstruction

DAS Filtering Requirements

Nyquist rate DAS



Oversampling rate DAS



Nyquist rate versus oversampling rate DAS

Nyquist rate DAS

Simple to implement

but

Quantisation noise is fixed

Requires higher order analogue LPF

Oversampling rate DAS

Adjustable random component of the quantisation noise (under some assumptions)

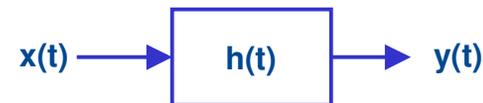
Requires lower order analogue LPF

but

Increased computational complexity

Loading effects introduced by filters

- Distortionless transmission through a filter
 - ✓ Constant magnitude spectrum (i.e. $|A(j\omega)|=K$)
 - ✓ Linear phase spectrum (i.e. $\theta(\omega)=-\omega t_0 \pm 2n\pi$)



- Convolution: Given $X(s)$ and $H(s)$ find $Y(s)$

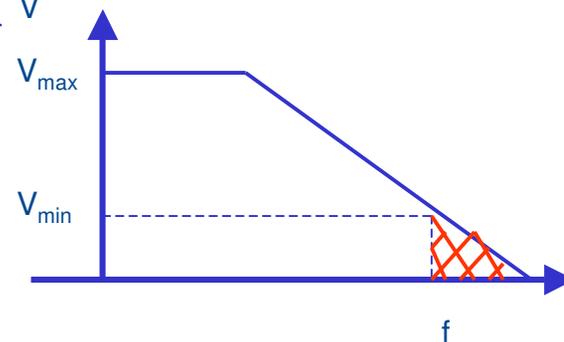
$$Y(s) = H(s) X(s)$$

$$y(t) = \int_{-\infty}^{+\infty} x(\tau) h(t-\tau) d\tau$$

- Deconvolution: Given $Y(s)$ and $H(s)$ find $X(s)$

$$X(s) = \frac{Y(s)}{H(s)}$$

$$x(t) = L^{-1} \left\{ \frac{Y(s)}{H(s)} \right\} v$$

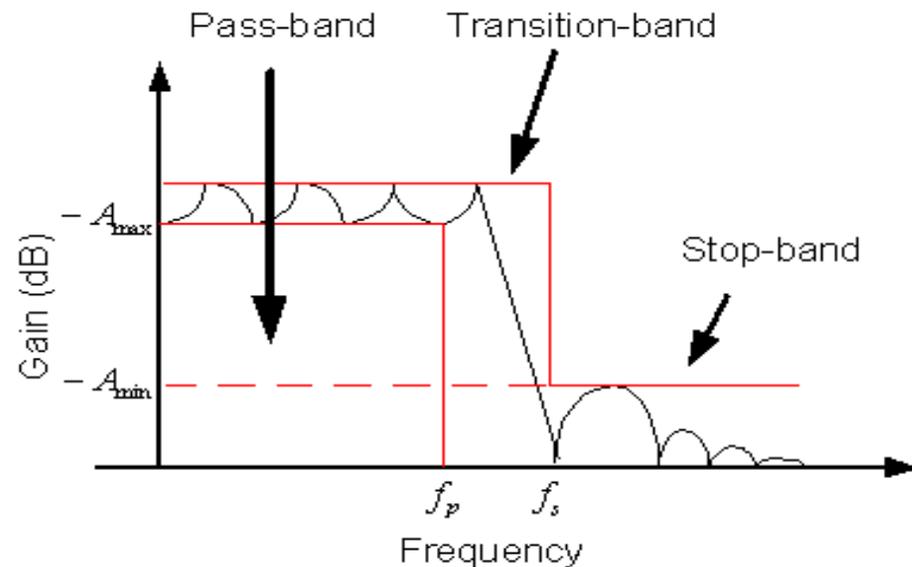


Choosing transfer function

- Butterworth, Chebyshev, Bessel, Inverse Chebyshev, ..., your own
 - Magnitude frequency response (monotonic, ripple)
 - Phase frequency response (linear, non-linear phase)
 - Different transfer function characteristic requires different order for a given specification
 - Not all filter topologies can realise all filter transfer functions

$$n_{but} = \frac{\log\left(\frac{10^{0.1A_{min}} - 1}{10^{0.1A_{max}} - 1}\right)}{2 \log\left(\frac{f_s}{f_p}\right)}$$

$$n_{che} = \frac{\cosh^{-1}\left(\frac{10^{0.1A_{min}} - 1}{10^{0.1A_{max}} - 1}\right)}{\cosh^{-1}\left(\frac{f_s}{f_p}\right)}$$



Choosing filter topology

- Popular circuit topologies
 - Sallen-Key, Multiple-loop feedback (Delyiannis -Friend), zero offset, state variable, ..., your own
- To choose the right circuit topology for an application check the:
 - ✓ Sensitivity of frequency response to component tolerance and temperature variation
 - ✓ Intrinsic noise (random)
 - ✓ DC offset (auto-zero?)
 - ✓ Number of components (cost)

DAS design example requirements

Specifications:

- Maximum signal frequency: 2.5kHz
- Quantisation error: 10ppm/FS
- Linearity: 10ppm/FS

Sampling rate: 120kHz

Filter order: 4, Butterworth transfer function (maximally flat)

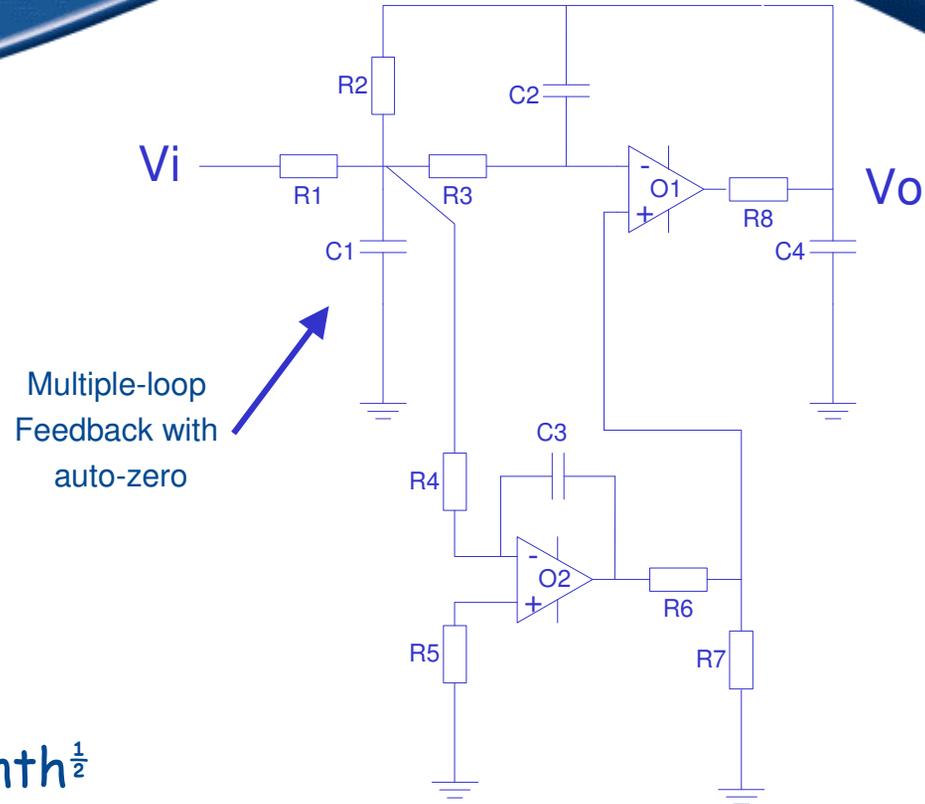
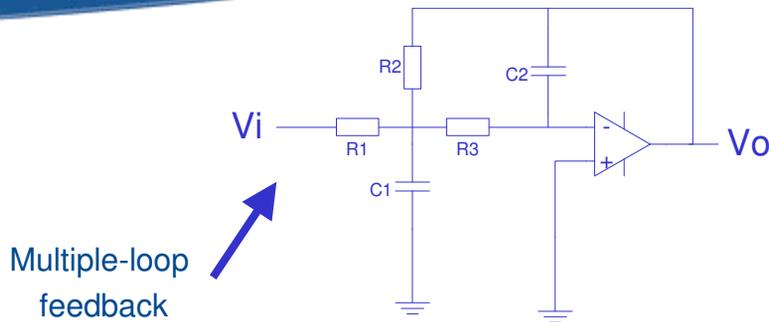
Cut-off frequency: 5kHz

Quantisation error: 1ppm/FS

DAS design example - topology selection

	Sallen-Key	Multiple-loop feedback	State variable
Sensitivity to component tolerance	✓	✓ ✓	✓ ✓ ✓
Intrinsic noise (random)	✓ ✓	✓	✓ ✓ ✓
DC offset	✓ ✓	✓ ✓ ✓	✓
Number of components	✓ ✓	✓ ✓ ✓	✓
Auto-zero?	No	Yes	No

DAS design example - transfer function realisation



- Low offset voltage
Typically $<10\mu\text{V}$
 $\Delta V_{\text{offset}} / \Delta T < 100\text{nV}/^\circ\text{C}$
 $\Delta V_{\text{offset/month}} < 50\text{nV/month}^{\frac{1}{2}}$
- Reduced $1/f$ noise
- Good AC linearity (better than 5ppm/FS)
- Relatively high frequency of operation (30kHz)
- Drive high capacitive load

How NPL can help you

- Calibration of DAS
 - DC and AC (<100kHz) calibration (e.g. accuracy, linearity)
 - 1/f noise measurements
- Design of DAS
 - Filters and signal conditioning
 - Sampling systems
 - Arbitrary waveform generators
- Aiming to calibrate ADC/DACs according to the IEEE Std 1241-2001

References

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MIT open course: <http://ocw.mit.edu/OcwWeb/Electrical-Engineering-and-Computer-Science/6-003Fall-2003/CourseHome/index.htm>