Monte Carlo Simulation of Scaling Effect on SEU and MBU Cross Sections by High Energy Protons

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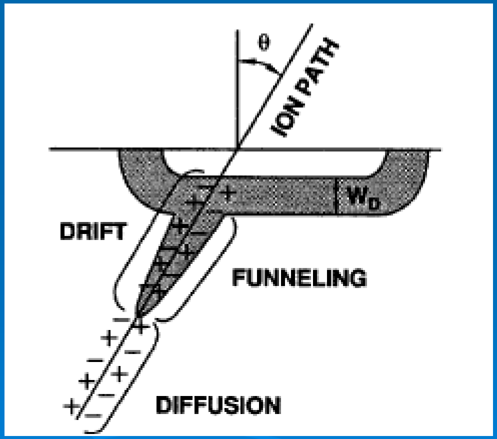
1. Introduction

- Radiation effects known as single-event upsets (SEU) in microelectronics have been recognized as a key reliability concern for many current and future silicon-based integrated circuit technologies.



- **Single Event Upset (SEU)**

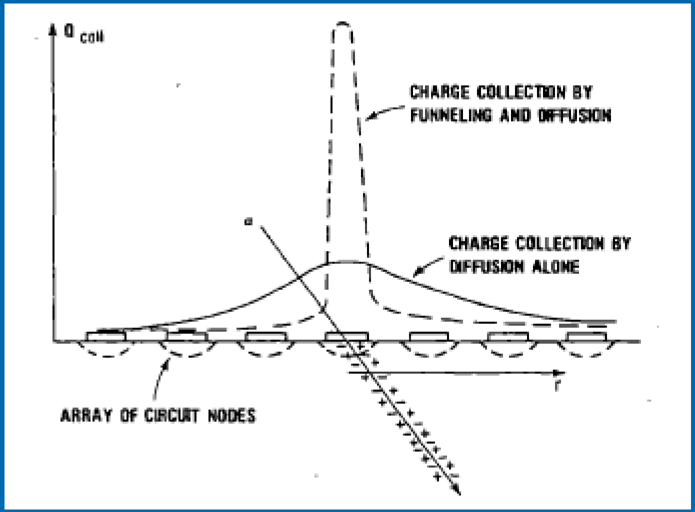
  Charge collection as a results of ionization interaction may cause change in circuit operation/or information stored (‘0’ to ‘1’ or ‘1’ to ‘0’) .

- **Multiple Bit Upset (MBU)**

  With the device downscaling, the physically adjacent bits can sometimes be upset by one particle known as multiple bit upset (MBU) .

  MBU has been shown to increase for smaller technologies

- Physics related to SEU phenomena
  - **proton-nucleus reactions**
  - **Secondary particles transport in device**
  - **Generation of electron-hole pairs**
  - **Charge collection**

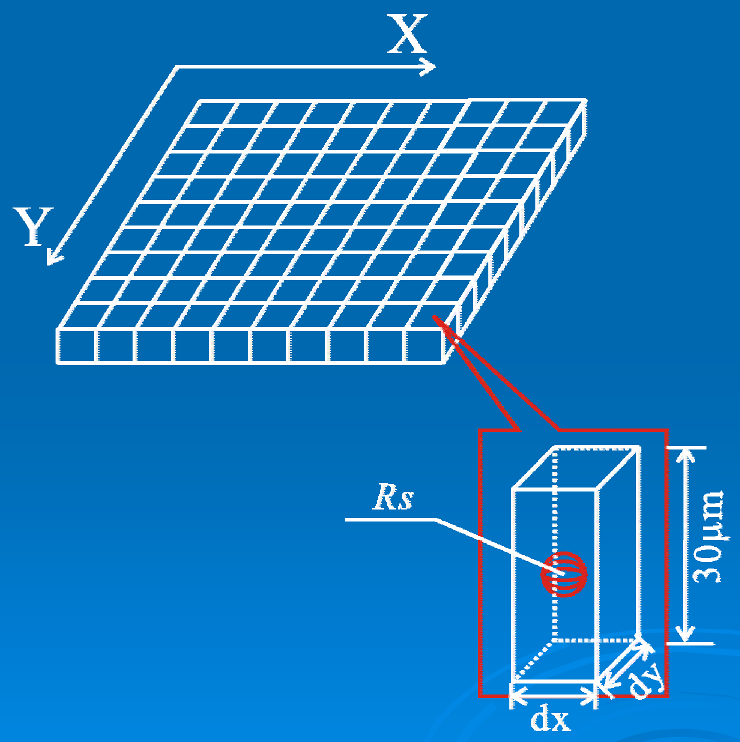


- The Monte Carlo simulation can provide insight into the details of nucleon strikes and device sensitivity

- In this paper, the Monte Carlo toolkits GEANT4 was used to study the single event effects (SEU and MBU) in three Static Random Access Memories (SRAM) devices with different dimensions induced by high energy protons. SEU and MBU cross sections were calculated to get their trends with device downscaling.

2. Modeling and Simulation Method

- Device Model



- The simplified model of device consists 128×128 memory cells, and each cell has a spherical sensitive volume with radius *Rs* in the center, and the thickness of cell is 30 µm . The material is simplified to be tread as pure ^{28}Si.

- Device scaling

Structure A Rs 0.710μm dx=dy=5μm; f = 1

Structure B Rs 0.568μm dx=dy=4μm; f =0.8

Structure C Rs 0.426μm dx=dy=3μm; f =0.6

- Proton induced spallation reactions
  - Proton-silicon reactions
  - Intranuclear cascade model
  - Secondary particles produced in device
  - Ionization energy deposition in sensitive volume
- Geant4 Monte Carlo simulation toolkit
  - Bertini intranuclear cascade model
  - Binary cascade
  - Forced collision

Force collision

Sample the position of reaction:

$$x = \xi_1 x_0$$

$$y = \xi_2 y_0$$

$$z = -\frac{1}{n\sigma_{in}} \ln\left[1 - \xi_3 (1 - e^{-n\sigma_{in} z_0})\right]$$

Reduced weight after reaction

$$W(z) = 1 - e^{-n\sigma_{in} z_0}$$

- Critical energy and Critical charge

The Ionization energy deposition in sensitive volume E is related to charges (Q) collected in the sensitive volume.

If Q > Qc, then SEU takes place. Q_C is the critical charge usually defined as the minimum amount of charge collection at a sensitive volume to cause a circuit upset.

$$E_C(\mathrm{MeV}) = 22.5Q_C(\mathrm{pC})$$

$$Q_C = \varepsilon(S/d)V_{dd} = \varepsilon SE$$

- Cross sections of single event upsets

$$\sigma_{SEU} = n_{Si}\sigma_{in}(E)V\varepsilon_{SEU}(E, E_C, V_s)$$

Here σ_{SEU} is the cross section of single event upsets, n_{Si} is atomic density of in silicon, $\sigma_{in}(E)$ is the inelastic cross section for the energy *E*, *V* is the volume of a memory cell, E_C is the critical energy, V_s is volume of sensitive area and

$$\varepsilon_{SEU} = \frac{\text{Number of single event upsets}}{\text{Number of particles induced}}$$

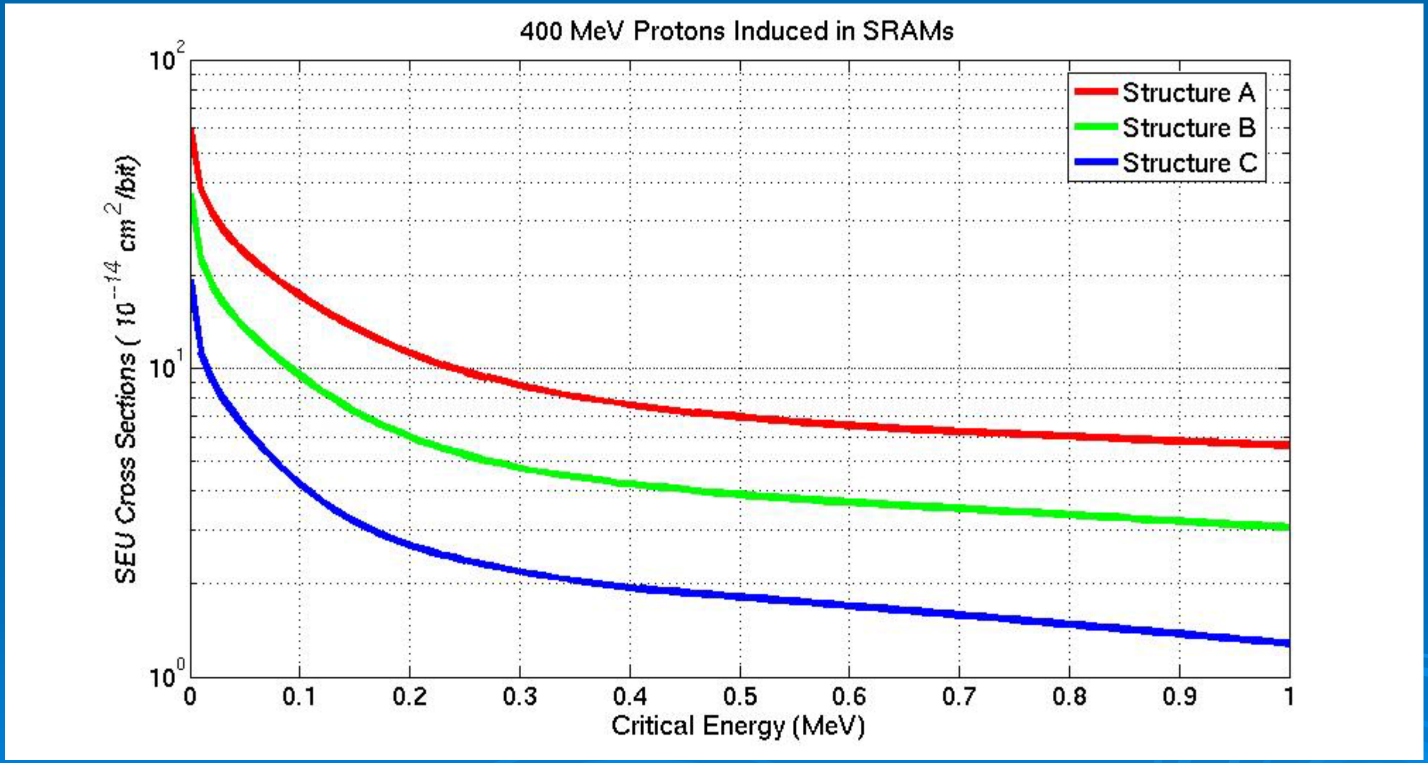
- Cross sections of multiple bit upsets

Cross sections of multiple bit upsets could be calculated by the same method with single event upsets:

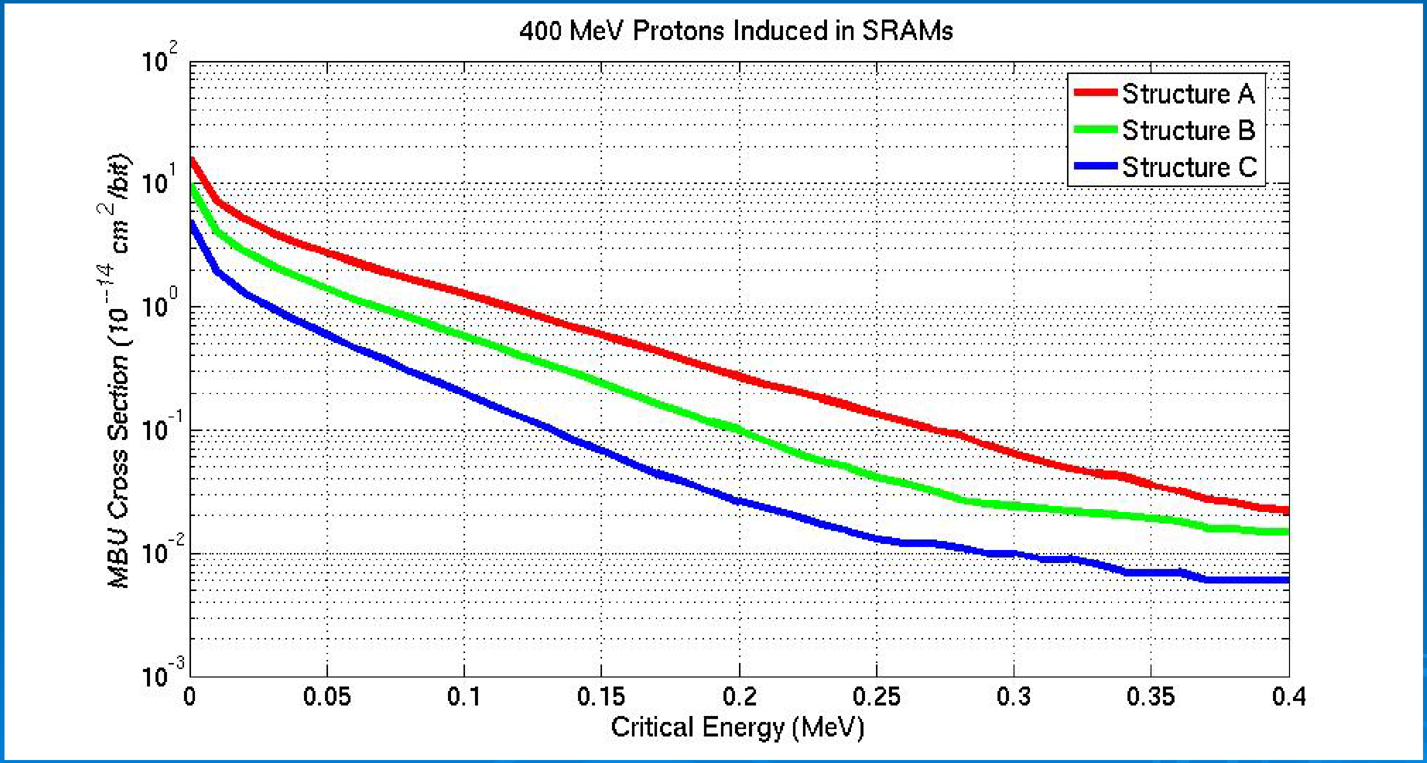
$$\sigma_{MBU} = n_{Si}\sigma_{in}(E)V\varepsilon_{MBU}(E, E_C, V_s)$$

3. Results and Conclusion

- SEU cross sections induced by 400 MeV protons



- MBU cross sections induced by 400 MeV protons



- The SEU and MBU cross sections decrease with the critical energy.
- And if the critical energy remains constant, they would be reduced with device downscaling.
- However, the critical energy may scale with law between f^2 to f^3.

- SEU cross sections with device downscaling

A	$8.7(\times10^{-14}cm^2/bit)$	
	If $Q_C \quad f^2$	*If* $Q_C \quad f^3$
B	6.2	7.2
C	3.9	5.8

- MBU cross sections with device downscaling

A	$6.4(\times10^{-16}cm^2/bit)$	
	If $Q_C \quad f^2$	*If* $Q_C \quad f^3$
B	13.4	25.6
C	15.9	46.7

The SEU cross section decreases slowly with device downscaling, but MBU cross section increases more quickly with device downscaling.

As shown in tables, the ratio of MBU to SEU is about 8% for structure C with f^3 law. For modern manufacture technologies, the MBU cross section should be few percent of the SEU cross section, and it can not be neglected.

The results help to predict the trends of evolutions of SEU and MBU cross sections for future technologies.

Thanks!