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Microelectronics *news*

Colin Lea (founder of the SSTC) receiving receiving congratulations from Chris Hunt (current SSTC manager).

Colin Lea:
A Man of Many Parts

The founder of the ***NPL Soldering Science and Technology Club*** (SSTC) and the champion of all the NPL studies of electronics interconnection, recently received a well-earned reception celebrating his 60th birthday and 33 years at NPL. Colin Lea joined NPL in 1971 as part of the reverse brain drain from America after two years at the University of Chicago, to work on the atomic structure of materials and interfaces. He quickly realised the enormous practical help NPL could give the electronics industry and so began his enduring and very successful involvement with the industry, with many significant landmarks along the way, including:

- formation of the SSTC, the first NPL industrial partnership club
- authorship of the industry standard book *A Scientific Guide to Surface Mount Technology* – over 2000 sold worldwide
- champion of the elimination of CFCs within the industry in the 1990s heyday of the CFC issue gave 80 talks a year around the world
- authorship of the industry standard book *After CFC? Options for Cleaning Electronic Assemblies*
- key player in the development of the SMART Group - he still manages its long-running European biennial meeting.
- a strong advocate for NPL's internationally recognised work in lead-free soldering

In a long and successful career Colin has received many accolades and awards. As early as 1979 he received The Metal Society Prize, and in 1995 was the first recipient of the ISHM (Hybrid Microelectronics) UK Awards for Professional Achievement. But the most important was the award of the OBE in 1994 for his work on CFC elimination. In America he received the prestigious EPA (Environmental Protection Agency) Stratospheric Protection Award, and in 1997 the EPA Best of the Best Award on the 10th anniversary of the Montreal Protocol. More recently his work was recognised by the United Nations Environmental Programme.

Anyone thinking that 33 years at NPL displays an unadventurous spirit should look at his passport. He has travelled widely through all the continents, often on solo treks "wandering like a tramp". He also played a pivotal role in running NPL's Children Party, and assembled a history of that event which lasted more than 80 years. As another one-off project, in 2000 Colin compiled a coffee-table book of the History of Materials Work at NPL, to mark 100 years of research.

This issue

Forthcoming Master Class 14 October 2004

The latest in the series of NPL Master Classes by world renowned speakers will be given by Dr Richard Ulrich (High Density Electronics Centre, University of Arkansas). Entitled *Embedded Passive Component Technology and Commercialisation*, the presentation will review potential applications, commercialised technology and future directions in components and processing.

NPL
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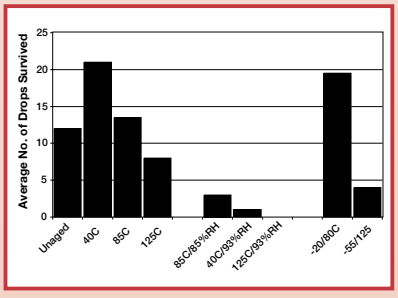
Partnership Opportunity – Performance of Conformal Coatings

Significant help in understanding how coatings protect electronics assemblies in aggressive environments, will soon be available to the industry via an exciting new collaborative 3-years project, sponsored by the DTI and with NPL and the Paint Research Association as major partners. The increasingly aggressive and diverse nature of the environments in which these assemblies must function reliably, whether the application be military, avionics, automotive, industrial control etc, is demanding of both materials and components. Consequently, industry is seeking more information to allow its engineers to differentiate between coatings, to predict their performances, and thereby have greater confidence in their use. The aims of this project, building on a previous, successful study, are to:

- identify potential protection mechanisms
- confirm the level of protection offered by coatings
- generate reliable test procedures
- develop more effective standards
- provide better specifications for conformal coatings
- acquire data leading to improved product design
- understand underlying degradation mechanisms

The project is in its final formulation stage, and interest in participation, or comments on its content, are welcomed.



Drop test results for BGAs and material A

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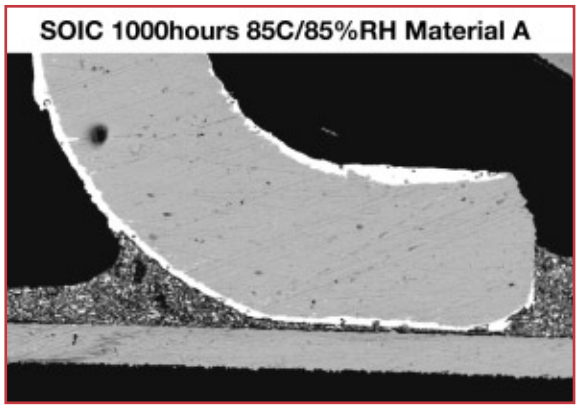
Test Refinements for Conducting Adhesives

Degradation of conducting adhesive (CA) joints appears to be moisture-driven rather than dependent on differences in thermal expansion coefficients. This is a major conclusion of the early work in the three-year DTI-sponsored collaborative project led by NPL and TWI into measurement methods for electrically conducting adhesives (see issue 18 – December 2003). Other main points from the work are:

- 85 °C/85%RH accelerated tests generated similar levels of degradation in the joints of a wide range of components, and is therefore recommended for use in stressing CA joints. Other tests were too harsh or more only appropriate for certain device types.



DC SIR behaviour for various test fluxes

- When joints began to fail electrically (lose continuity) they remained mechanically sound (shear data). Hence mechanical testing for joint evaluation can provide misleading information, and electrical testing is recommended.
- Joints failing mechanically showed little evidence of inter-material failure.
- Not surprisingly, resistance to mechanical shock of the CA joints was significantly lower than that afforded by solder alloys. When assemblies were dropped 1.5 m onto solid metal surfaces, whilst the smaller components (e.g. chip resistors) remained unaffected the larger components (e.g. QFPs) became detached. A secondary coating did alleviate this problem, but the test proved of little use in differentiating between stress regimes.
- TWI tests involved flip-chips on FR4 substrates with anisotropic CA joints, and it was encouraging that a pattern of behaviour similar to that observed by NPL with the isotropic CAs, was recorded.

The next phase will study the effects of component and substrate finishes on the joint characteristics.

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Reliability: the Main Issue for Lead-free

Although the 90 attendees at the winter SSTC meeting were left in no doubt that joint reliability is the major issue for those implementing lead-free soldering technology, the speakers were all optimistic that the issues would be successfully addressed by the July 2006 deadline. David Andrew Lunnon (DTI) indicated that the "fine tuning" of the legislation is nearing completion providing a clearer view of what would be required of industry. Martin Wickham (NPL) reviewed suppliers' information and published data on reliability issues from lead contamination in solder joints, whilst Bob Willis (EPS) provided graphic evidence of the practical effects of secondary reflow of lead-free joints with components having SnPb terminations. The value in assessing the reliability of lead-free solder joints using accelerated thermal cycling followed by shear strength measurements was promoted by Milos Dusek (NPL). Rachel Thomson (Loughborough University) ably demonstrated the usefulness of current thermodynamic and kinetic modelling in understanding the new soldering process and in predicting microstructural changes in service.

Three NPL speakers considered other aspects of implementing lead-free soldering: the occurrence of voiding and its effect on the reliability of lead-free joints, measuring tin whisker propensity, susceptibility of PWB substrates to CAF growth. The proceedings of the entire meeting (£50) are now available.

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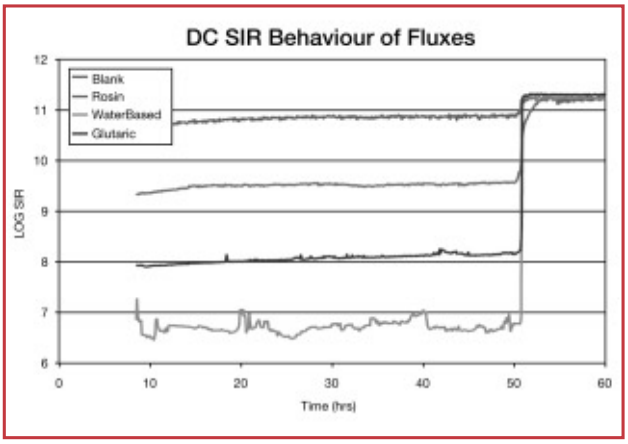
AC Conditions Affect SIR Measurements

The demonstration that SIR results on assembled boards are greatly influenced by whether the driving voltage is AC or DC driven, provides a major step in understanding the effects of contamination on board reliability under different service conditions (see issue 17 – June 2003). In reality the majority of electronic designs incorporate at least some AC or digital functionality.



DC SIR behaviour for various test fluxes

The work involved measuring the effects on SIR of various flux contaminations (rosin, water-based no-clean, glutaric acid in IPA, control) when exposed to harsh environments and an AC electrical environment. Boards were baked for 5 mins at 100 °C, and an impedance analyser used to monitor the board response across the frequency range 1 KHz - 100 KHz. Salient findings were:

- Not only were the SIR behaviours markedly different under DC and AC conditions for each flux, but the ranking of the fluxes was also different.
- The key factor is the interaction between moisture and flux, to which the AC approach appears more sensitive (e.g. at 100 KHz there is minimal change in impedance with humidity; at 2 KHz the impedance changes by ~85%).
- The higher the frequency the lower was the impedance, and the changes in impedance may be enough to affect circuit functionality.
- Changes in some of the properties measured were outside the tolerances set for some components.

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NPL Attracts Highest Attendence

At *Southern Manufacturing 2004*, UK's largest regional manufacturing technology, electronics and subcontracting exhibition, (Thorpe Park 18/19.2.04), NPL achieved the highest attendance figures in the electronics section with its session on lead-free soldering technology. The high attendance confirmed that lead-free soldering remains *the* "hot topic". The subjects covered included soldering at high temperatures, reliability, component robustness, different materials, and supply chain issues of responsibility and integrity. Of particular interest was the session entitled "*Are your process residues at an acceptable level?*"

NPL Delivers Lead-free Soldering Seminars

Lead-free soldering is now a reality for electronics manufacturers, and with legislation in place the clock is ticking and manufacturers and users alike are now feeling the need to react, but in many cases are not sure of the appropriate actions. In response NPL has delivered, and continues to offer, a series of seminars designed for those keenly concerned with practical issues of implementation that have financial, legal and reliability implications. Each attendee receives a copy of the *NPL Lead-free Assembly and Soldering Cookbook 3*, worth £100. The seminars are tailored for management, design, procurement, quality and process engineers, and further information can be obtained from a 2004 Workshop Brochure downloaded from **www.npl.co.uk/ei/documents/leadfreemaster2004.pdf.**

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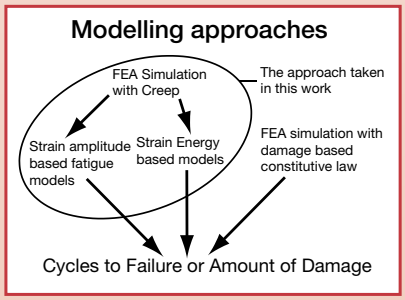
Modelling Provides an Insight

The ability to understand the mechanical properties of solder joints has been given a boost by the new application of modelling techniques in a NPL-Greenwich University collaborative programme. Being able to understand how damage accumulates within the solder, and how this damage affects the strength of the joints, is vital to industry for design, process control and reliability assessment. Two approaches of such modelling have been successfully developed to describe the degradation in shear strength of lead-free solder joints.

In the first, a linear multiple regression method has been used to predict the degree of damage (and hence reliability) after cycling SM resistors through one of six thermal cycling regimes. The results suggest that the composition of the solder itself (SnAg or SnAgCu) has a negligible effect on the level of damage. By contrast the size of the joint does have a significant effect on the damage accumulation, larger joints being stronger.

A second technique, based on FEA (finite element analysis), has been used to study damage accumulated in joints during each cycle. The damage is strongly dependent on location in the joint, and the model can predict both local damage and ensuing crack path. Extensive microsectioning has been used to validate the model, which indicates where damage occurs in the joint, and when it occurs during the thermal cycle. Hence the cycling regime can be tailored for particular damage generation. For example, the time spent at the low temperature dwell does not significantly contribute to damage, and can be minimised or omitted to reduce the test period.



FEA modelling approaches

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NPL Reports Now Available

Good Practice Guide

- Solderability testing of surface mount components and PCB pads - No.66

NPL Reports

- Developing a test method to characterise internal stress in tin coatings: Phase 1 - MATC(A)148
- Crack detection methods for lead-free solder joints - MATC(A)164
- The impact thermal cycling regime on the shear strength of lead-free solder joints - MATC(A)156
- Influence of stencil and aperture design on fine pitch printing for various solder paste types - MATC(A)145
- CAF susceptibility of PWB substrates - MATC(A)155

You can download these reports FOR FREE directly from:

http://libsvr.npl.co.uk/npl_web/search.htm

Any comments and views on this newsletter, or requests for further copies should be addressed to:

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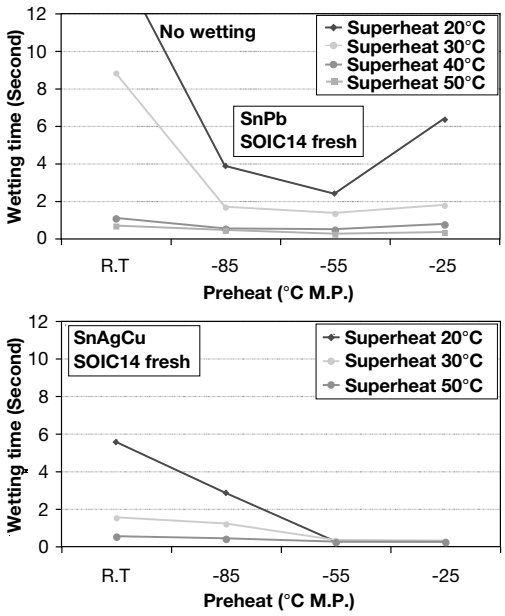
Solderability Pre-heating Worries Overcome

A refinement of the widely used solderability technique now permits measurements under conditions which closely mimic those of industrial soldering, thereby providing greater credibility for the solderability data. Some parts of industry have been concerned that whereas the soldering process invariably involves gradual heating of the components to the soldering temperature (210 °C), solderability testing is always performed on cold components, and hence a test temperature of 235 °C is required. With its industrial partner, Concoat, NPL has now developed a controlled pre-heating arrangement for solderability testing using an IR system, which can deliver the same temperature profile to the test component as that used in electronics assembly. This development may result in modifications to the standard test procedure.



Wetting time with pre-heat temperature for SOIC14 devices

The pre-heat system allows a reduction in the necessary superheat, and hence in the test temperature, to a value closer to that of actual soldering. Trials have confirmed that good wetting can be achieved with only 30 degrees superheat for SnPb solder and components with a variety of finishes, giving a test temperature of 213 °C, typical of reflow processes. This advantage will be vital for testing lead-free solders having higher soldering temperatures - for SnAgCu solder a superheat of only 20 degrees is sufficient. Other results have confirmed that, due to flux volatilisation, high pre-heat temperatures do not always give the shortest wetting time.

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WEEE/ROHS Legislation Update

As July 2006 nears, the position regarding these two pieces of legislation becomes clearer, especially regarding the collection, treatment and disposal of WEEE. But there are still several questions to be settled. The government is undertaking a consultation process on its preferred option for implementing both Directives, which involves a "clearing house" to coordinate collection of WEEE nationwide for treatment and recovery. The details and background of this option, and other relevant documents, are available on **www.dti.gov.uk/sustainability/weee**. As far as lead in solders is concerned, the position has hardly changed. Lead in solder is still included in the ROHS ban, and the maximum level of lead allowable in homogeneous materials is 0.1% by weight, although a precise definition of a homogeneous material has not yet been provided. Worries concerning labelling requirements are also increasing. But what appear to be emerging as industry's main concern are *transition issues*, in particular, where does the responsibility lie for eliminating lead from EEE? Responding to these worries NPL has been commissioned by a number of organisations to give independent, on-site, company-specific seminars aimed at raising the awareness at all levels within that company, addressing its supply chain issues and suggesting appropriate plans/strategies.

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